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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,355	07/03/2003	Aryan Saed	11178-7	7281

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EXAMINER	
WILLIAMS, LAWRENCE B	
ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 12/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,355	SAED ET AL.	
	Examiner	Art Unit	
	Lawrence B. Williams	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) *1, 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. This application has been filed with informal drawings, which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Objections

4. Claim 1 is objected to because of the following informalities: The examiner suggests "said signal processing system" in line 11 of the claim.

Appropriate correction is required.

5. Claim 17 is objected to because of the following informalities: The examiner suggests applicant replace the word "bases" with "based" in line 2 of the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 5, 9-11, 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Faulkner et al. (Adaptive Linearization Using Predistortion- Experimental Results).

(1) With regard to claim 1, Faulkner et al. discloses in Fig. 2, a system for processing an input signal (m), the system comprising: a predistortion subsystem (H_R , H_θ , adapt) for receiving said input signal and for producing a predistorted signal by applying a deliberate predistortion to said input signal; and a signal processing subsystem (RF section; pg. 323, col. 2, line 46- pg. 324, col. 1, line 2), receiving and processing said predistorted signal and producing a system output signal, wherein said predistortion subsystem distorts said input signal to compensate for distortions in said system output signal (pg. 324, col. 1, lines 9-11); said signal processing subsystem decomposes said predistorted signal into separate components, each of said separate components being processed separately (RF section shows signal (m) decomposed into two signal components with individual processing); and said processing subsystem

combines (combiner, ⊕) said components after processing to produce said system output signal.

(2) With regard to claim 2, Faulkner et al. also discloses in Fig. 2, a system according to claim 1 wherein said signal processing subsystem comprises: a signal decomposer (D/A) for decomposing said predistorted signal into at least two components (as shown in Fig. 2, the D/A serves to decompose the predistorted signal into at least two components); at least two signal component processor blocks (filter and block s; filter and block c) each signal processor block receiving an output of said signal decomposer and each signal processor block separately processes said output received from said signal decomposer; and a combiner (⊕) receiving a processed output from each of said at least two signal component processor blocks, said combiner producing said system output signal from said processed outputs of said at least two signal component processor blocks.

(3) With regard to claim 3, Faulkner et al. also discloses a system according to claim 2 wherein at least one of said at least two signal component processor blocks includes an amplifier (pg. 323, col. 2, line 46-pg. 324, col. 1, line 2).

(4) With regard to claim 5, Faulkner et al. also discloses a system according to claim 1 wherein said system is part of a signal transmission system (pg. 323, col. 1, line 1).

(5) With regard to claim 9, Faulkner et al. also discloses a system according to claim 1 wherein said deliberate predistortion includes magnitude distortions which adjust a magnitude of said input signal (pg. 323, col. 2, lines 35-38).

(6) With regard to claim 10, Faulkner et al. also discloses a system according to claim 1 wherein said deliberate predistortion includes phase distortions which adjust a phase of said input signal (pg. 323, col. 2, lines 38-40).

(7) With regard to claim 11, Faulkner et al. also discloses a system according to claim 1 wherein said deliberate predistortion is based on at least one entry in a lookup table (pg. 323, col. 2, lines 35-40).

(8) With regard to claim 19, Faulkner et al. also discloses a system according to claim 11 wherein said deliberate predistortion is based on an interpolation of entries in said table (pg. 324, col. 2, lines 28-35).

8. Claims 12-15, 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Faulkner et al. (Adaptive Linearization Using Predistortion- Experimental Results).

(1) With regard to claim 12, Faulkner et al. discloses in Fig. 2, a method for processing an input signal (m) to produce a system output signal, the method comprising: receiving said input signal; applying a deliberate predistortion (H_R , H_θ , adapt) to said input signal to result in a predistorted signal; decomposing said predistorted signal into at least two components signals (RF section shows signal (m) decomposed into at least two component signals); combining ($\oplus$) said at least two components signals to produce said system output signal.

(2) With regard to claim 13, Faulkner et al. discloses a method according to claim 12 wherein said system output signal is an RF modulated version of said input signal (pg. 323, col. 2, line 46-pg. 324, col. 1, line 2).

(3) With regard to claim 14, Faulkner et al. also discloses a method according to claim 12 further including a processing step of separately processing each of said at least two component signals prior to step d). (Fig. 2 discloses at least two signal component processor blocks (filter and block s; filter and block c) for separately processing each of the two signal components before the step of combining.

(4) With regard to claim 15, Faulkner et al. also discloses a method according to claim 14 wherein said processing step includes amplifying at least one of said at least two component signals (pg. 323, col. 2, line 46-pg. 324, col. 1, line 2).

(5) With regard to claim 17, Faulkner et al. also discloses a method according to claim 12 wherein step a) further includes the step of accessing an entry in a lookup table, said deliberate predistortion being bases on said entry (pg. 323, col. 2, lines 35-40).

(6) With regard to claim 18, Faulkner et al. also discloses a method according to claim 17 wherein said deliberate predistortion is based on an interpolation of entries in said table (pg. 324, col. 2, lines 28-25).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over by Faulkner et al. (Adaptive Linearization Using Predistortion- Experimental Results) as applied to claim 3 above, and further in view of Cox (Linear Amplification with Nonlinear Components).

As noted above, Faulkner et al. discloses all limitations of claim 4 above. Faulkner et al. does not teach the system of claim 3, wherein the amplifier is a non-linear amplifier.

However, Cox teaches Fig. 1, a LINC amplifier for separating a signal into components wherein the amplifiers (G) are non-linear amplifiers (pg. 1942, col. 2, lines 10-11).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Cox for the amplifiers in the subsystem of Faulkner et al. because of their readily availability over linear amplifiers (pg. 1942, col. 1, lines 8-21).

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Faulkner et al. (Adaptive Linearization Using Predistortion- Experimental Results) as applied to claim 1 above, and further in view of Wright et al. (US Patent 5,990,738).

As noted above, Faulkner et al. discloses all limitations of claim 1. Faulkner et al. does not teach the system according to claim 1, wherein at least some of said distortion are due to said combiner.

However, Wright et al. teaches a compensation system and method for a linear power amplifier wherein at some of the distortion compensated for are due to the combiner (abstract; col. 3, lines 39-50; col. 5, lines 65-67).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Wright et al. as a method of compensating for differences in the characteristics

of the separate signal paths which would cause the combination not to accurately represent the original signal (abstract).

12. Claims 7 and 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Faulkner et al. (Adaptive Linearization Using Predistortion- Experimental Results) as applied to claim 3 above, and further in view of Applicant's Admitted Prior Art.

(1) With regard to claim 7, as noted above, Faulkner et al discloses all limitations of claim 3. However, Faulkner et al. does not teach the system according to claim 3 wherein said amplifier is a switch mode amplifier. However Applicant's Admitted prior art teaches the Chireix amplifier subsystem wherein the amplifier is a switch mode amplifier (pg. 10, paragraph [00031].

Therefore it would have been obvious to one skilled in the art at the time of invention to incorporate the use of a switch mode amplifier in the system of Faulkner et al. to provide low output impedances that allow for higher amplification efficiencies in the system.

(2) With regard to claim 8, Applicant's admitted prior art also teaches wherein the amplifier has a low output impedance.

Therefore it would have been obvious to one skilled in the art at the time of invention to incorporate the use of an amplifier with low output impedance in the system of Faulkner et al. to provide for higher amplification efficiencies in the system.

13. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Faulkner et al. (Adaptive Linearization Using Predistortion- Experimental Results) as applied to claim 14 above, and further in view of Gu (US Patent 6,737,914 A1).

As noted above, Faulkner et al. discloses all limitations of claim 14. Faulkner et al. does not explicitly teach wherein the processing step includes phase modulating at least one of said at least two component signals.

However, Gu teaches in Fig. 1, an amplifier subsystem wherein decomposed signal components are phase modulated (elements 104, 106).

Therefore it would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Gu to remove the effects of phase and gain mismatches in order to improve the accuracy of the combined signal components (col. 2, lines 16-51).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.) Birafane et al. discloses in IEEE Transactions on Microwave Theory and Techniques, Phase-Only Predistortion for LINC Amplifiers with Chivereix-Outphasing Combiners.

b.) Kolanek discloses in US 6,147,533 Amplification Using Amplitude Reconstruction of Amplitude and/or Angle Modulated Carrier.

c.) Kolanek discloses in US Patent 6,215,354 B1 Closed Loop Calibration for an Amplitude Reconstruction Amplifier.

d.) Kolanek discloses in US 2002/0047745 A1 Management of Internal Signal Levels and Control of the Net Gain for an LINC Amplifier.

e.) Saed et al. discloses in US Patent 7,068,101 B2 Adaptive Predistortion for a Transmit System.

f.) Saed discloses in US 2006/0109052 A1 Adaptive Predistortion for a Transmit System.

g.) Saed discloses in US 20065/0003770 A1 Predistortion Circuit for a Transmit System.

h.) Saed discloses in US Patent 6,975,162 B2 Adaptive Predistortion for a Transmit System with Gain, Phase and Delay Adjustments.

i.) Saed discloses in US Patent 7,034,613 B2 Adaptive Predistortion for Transmit System with Gain, Phase and Delay Adjustments.

j.) Saed discloses in US Patent 7,015,752 B2 Adaptive Predistortion for a Transmit System with Gain, Phase and Delay Adjustments.

k.) Saed discloses in US Patent 7,026,872 B2 Adaptive Predistortion for a Transmit System with Gain, Phase and Delay Adjustments.

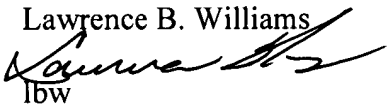
l.) Saed discloses in US Patent 7,026,871 B2 Adaptive Predistortion for a Transmit System.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ghayour Mohammad can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams



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December 10, 2006